IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PACT XPP TECHNOLOGIES, AG, Plaintiff,	§ §	
v.	§ §	CIVIL ACTION NO. 2-07cv563-CE
XILINX, INC. & AVNET, INC., et al. Defendants.	§ §	

MEMORANDUM OPINION AND ORDER

I. INTRODUCTION

Plaintiff PACT XPP Technologies AG's ("Plaintiff") filed suit on April 11, 2008, alleging that Defendants Xilinx, Inc. and Avnet, Inc. (collectively "Defendants") infringe Plaintiff's U.S. Patent No. 5,943,242 ("the '242 Patent"), U.S. Patent No. 6,859,869 ("the '869 Patent"), U.S. Patent No. 6,728,871 ("the '871 Patent"), U.S. Patent No. 7,237,087 ("the '087 Patent"), U.S. Patent No. 6,119,181 ("the '181 Patent"), U.S. Patent No. 6,513,077 ("the '077 Patent"), U.S. Patent No. 6,338,106 ("the '106 Patent"), U.S. Patent No. 6,088,795 ("the '795 Patent"), U.S. Patent No. 7,028,107 ("the '107 Patent"), U.S. Patent No. 6,542,998 ("the '998 Patent"), and U.S. Patent No. 6,526,520 ("the '520 Patent") (collectively "the patents-in-suit"). On February 22, 2011, the Court held a claim construction hearing where the parties presented oral arguments regarding the disputed terms. This order will first briefly address the technology at issue in the case and then turn to the merits of the claim construction issues.

II. BACKGROUND OF THE TECHNOLOGY

The eleven patents-in-suit claim aspects of reconfigurable computing. Some of the asserted patents claim processors with processing array elements that can be "dynamically reconfigured." Generally speaking, dynamic reconfiguration is the process of taking a group of processing array elements that are operating with a first configured function and interconnection, and changing the function and interconnection of these elements to operate with a second configured function. Importantly, the reconfiguration of these elements occurs without affecting the other processing array elements, which continue processing data according to their configured function. In contrast, the prior art reconfigurable processors required the processor to stop processing data and reconfigure all the processing array elements as a group. The dynamically reconfigurable architectures disclosed in the patents provide a different approach that is purported to be faster and more flexible.

The patents-in-suit also disclose a bus system within a reconfigurable processor that provides communication with external devices. Early reconfigurable processors required many of the processing array elements to be configured as "glue logic" that translated the internal signals generated by one external device into output formats understandable to other external devices, and vice-versa. The patents-in-suit remedy this inefficiency with a dedicated "interface unit" that forms a bus system and controls the communications between the processor and external devices. This frees many of the processing array elements within the processor to perform computations or to implement other aspects of the application design.

The eleven patents-in-suit can be divided into five families. In general, each member of a family shares a common specification. All of the patents-at-issue, except for the '242 patent and

the ‘869 patent, include a glossary of terms at the end of the specification. The breakdown of the patent families is as follows:

Technology	Patents
Dynamically reconfigurable data processing system	U.S. Patent No. 5,943,242 (“the ‘242 Patent”) U.S. Patent No. 6,859,869 (“the ‘869 Patent”)
Runtime configurable arithmetic and logic cell	U.S. Patent No. 6,728,871 (“the ‘871 Patent”) U.S. Patent No. 7,237,087 (“the ‘087 Patent”)
I/O and memory bus system for DFPs and units with two- or multi-dimensional programmable cell architectures	U.S. Patent No. 6,119,181 (“the ‘181 Patent”) U.S. Patent No. 6,513,077 (“the ‘077 Patent”) U.S. Patent No. 6,338,106 (“the ‘106 Patent”)
Process for automatic dynamic reloading of data flow processors (DFPs) and units with two or three-dimensional programmable cell architectures (FPGAs, DPGAs and the like)	U.S. Patent No. 6,088,795 (“the ‘795 Patent”) U.S. Patent No. 7,028,107 (“the ‘107 Patent”)
Method of self-synchronization of configurable elements of a programmable module	U.S. Patent No. 6,542,998 (“the ‘998 Patent”) U.S. Patent No. 6,526,520 (“the ‘520 Patent”)

The abstract for the ‘242 patent (first family) states:

> A data processing system, wherein a data flow processor (DFP) integrated circuit chip is provided which comprises a plurality of orthogonally arranged homogeneously structured cells, each cell having a plurality of logically same and structurally identically arranged modules. The cells are combined and facultatively grouped using lines and columns and connected to the input/output ports of the DFP. A compiler programs and configures the cells, each by itself and facultatively grouped, such that random logic functions and/or linkages among the cells can be realized. The manipulation of the DFP configuration is performed during DFP operation such that modification of function parts (MACROs) of

the DFP can take place without requiring other function parts to be deactivated or being impaired.

As an exemplary claim of the first family, Claim 1 of the ‘242 patent is reproduced below:

> 1. A data processing system for manipulating data, comprising:
> an integrated circuit data flow processor, said data flow processor including a plurality of cells arranged in a pattern having two or more dimensions, a plurality of connecting lines disposed between each said cells and a plurality of input and output ports, said cells connected to neighboring cells by a plurality of first data connections, said cells also connected to said connecting lines by a plurality of second data connections, at least some of said cells being selectively configured to perform a first function, the at least some of said cells being selectively reconfigured to perform a second function, the second function being different than the first function, the at least some of said cells being selectively grouped with another of said cells into functional parts by means of said first and second data connections to perform a third function, the at least some of said cells being selectively regrouped to perform a fourth function, the fourth function being different than the third function, said cells connected to said input and output ports;
> a timer arrangement coupled to at least one of the functional parts and including at least one of a state machine and a counter, the timer arrangement synchronizing data processing by the at least one of the functional parts and generating synchronization signals; and
> a compiler configuring and reconfiguring selected ones of the at least some of said cells and selectively grouping and regrouping said selected ones of the at least some of said cells into functional parts as a function of the synchronization signals providing various logic functions and data manipulations among said cells and said functional parts to be realized, said compiler reconfiguring and regrouping said selected ones of the at least some of said cells during operation of said data flow processor while simultaneously others of the at least some of said cells not being reconfigured or regrouped process data.

The abstract for the ‘871 patent (second family) states:

> A cascadable arithmetic and logic unit (ALU) which is configurable in function and interconnection. No decoding of commands is needed during execution of the algorithm. The ALU can be reconfigured at run time without any effect on surrounding ALUs, processing units or data streams. The volume of configuration data is very small, which has positive effects on the space required and the configuration speed. Broadcasting is supported through the internal bus systems in order to distribute large volumes of data rapidly and efficiently. The ALU is equipped with a power-saving mode to shut down power consumption completely. There is also a clock rate divider which makes it possible to operate the ALU at a slower clock rate. Special mechanisms are available for feedback on the internal states to the external controllers.

As an exemplary claim of the second family, Claim 4 of the '871 patent is reproduced below:

> 4. A circuit, comprising:
> a plurality of coarse grained processing array elements;
> a primary logic unit communicatively coupled to the processing array elements; and
> an internal bus system;
> wherein each of the processing array elements is reconfigurable at a run time without effecting other processing array elements and without effecting data streams communicated between transmitters and receivers, by selecting one of a set of predefined, non-alterable instructions according to configuration data sent from the primary logic unit and addressed to the processing array element, and each of the processing array elements is decoupled from the internal bus system.

The abstract for the '181 patent (third family) states:

> A uniform bus system is provided which operates without any special consideration by a programmer. Memories and peripheral may be connected to this bus system without any special measures. Likewise, units may be cascaded with the help of the bus system. The bus system combines a number of internal lines, and leads them as a bundle to terminals. The bus system control is predefined and does not require any influence by the programmer. Any

number of memories, peripherals or other units can be connected to the bus system.

As an exemplary claim of the third family, Claim 1 of the ‘181 patent is reproduced below:

> 1. A bus system, comprising:
> a processing unit, the processing unit having a multi-dimensional programmable cell architecture;
> a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled;
> at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device; and
> at least one state machine for controlling the at least one interface unit.

The abstract for the ‘795 patent (fourth family) states:

> A method for processing data in a configurable unit having a multidimensional cell arrangement a switching table is provided, the switching table including a controller and a configuration memory. Configuration strings are transmitted from the switching table to a configurable element of the unit to establish a valid configuration. A configurable element writes data into the configuration memory. The controller of the switching table recognizes individual records as commands and may execute the recognized commands. The controller may also recognize and differentiate between events and execute a action in response thereto. In response to an event, the controller may move the position of a pointer, and if it has received configuration data rather than commands for the controller, sends the configuration data to the configurable element defined in the configuration data. The controller may send a feedback message to the configurable element. The configurable element may recognize and analyze the feedback message. An configurable element may transmit data into the configuration memory of the switching table.

As an exemplary claim of the fourth family, Claim 8 of the ‘795 patent is reproduced below:

> 8. A method for dynamically reconfiguring a configurable unit, the configurable unit including a plurality of configurable elements and having a multidimensional cell arrangement, the method comprising the steps of:
>
> storing in a table configuration strings;
>
> detecting an event;
>
> transmitting a selected one of the configuration strings from the table to at least one of the plurality of configurable elements in response to the detection of the event, the selected one of the configurations strings being selected as a function of the detected event;
>
> receiving, by the at least one of the plurality of configurable elements, the transmitted configuration string; and
>
> changing a configuration of the at least one of the plurality of configurable elements as a function of the received configuration string.

The abstract for the ‘989 patent (fifth family) states:

> A method which permits self-synchronization of elements to be synchronized. Synchronization is neither implemented nor managed by a central entity. By shifting synchronization into each element, more synchronization tasks can also be performed simultaneously, because independent elements no longer interfere with one another when accessing the central synchronization entity. In a module with a two- or multi-dimensionally arranged programmable cell structure, each configurable element can access the configuration and status register of other configurable elements over an interconnecting structure and thus can have an active influence on their function and operation. The configuration can thus be accomplished by a load logic from a processing array.

As exemplary claims of the fifth family, Claims 1 and 15 of the ‘795 patent are reproduced below:

> 1. A method for synchronization of data processing sequence control in a system with a plurality of configurable elements arranged in a programmable cell structure, comprising:

generating a synchronization signal during processing by a first configurable processing element;
sending the synchronization signal to a second configurable processing element over a bus system; and
synchronizing data processing in the second configurable processing element using the synchronization signal.

15. The method according to claim 1, further comprising:
broadcasting the synchronization signal to a plurality of configurable processing elements.

III. GENERAL PRINCIPLES GOVERNING CLAIM CONSTRUCTION

"A claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999). Claim construction is an issue of law for the court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996).

To ascertain the meaning of claims, the Court looks to three primary sources: the claims, the specification, and the prosecution history. *Markman*, 52 F.3d at 979. The specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. *Id.* A patent's claims must be read in view of the specification, of which they are a part. *Id*. For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *Id*. "One purpose for examining the specification is to determine if the patentee has limited the scope of the claims." *Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000).

Nonetheless, it is the function of the claims, not the specification, to set forth the limits of the patentee's invention. Otherwise, there would be no need for claims. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). The patentee is free to be his own

lexicographer, but any special definition given to a word must be clearly set forth in the specification. *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1388 (Fed. Cir. 1992). Although the specification may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. *Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994).

This Court's claim construction decision must be informed by the Federal Circuit's decision in *Phillips v. AWH Corporation*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). In *Phillips*, the court set forth several guideposts that courts should follow when construing claims. In particular, the court reiterated that "the *claims* of a patent define the invention to which the patentee is entitled the right to exclude." 415 F.3d at 1312 (emphasis added) (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To that end, the words used in a claim are generally given their ordinary and customary meaning. *Id*. The ordinary and customary meaning of a claim term "is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id*. at 1313. This principle of patent law flows naturally from the recognition that inventors are usually persons who are skilled in the field of the invention and that patents are addressed to and intended to be read by others skilled in the particular art. *Id*.

The primacy of claim terms notwithstanding, *Phillips* made clear that "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id*. Although the claims themselves may provide guidance as to the meaning of

particular terms, those terms are part of "a fully integrated written instrument." *Id*. at 1315, *quoting Markman*, 52 F.3d at 978. Thus, the *Phillips* court emphasized the specification as being the primary basis for construing the claims. *Id*. at 1314-17. As the Supreme Court stated long ago, "in case of doubt or ambiguity it is proper in all cases to refer back to the descriptive portions of the specification to aid in solving the doubt or in ascertaining the true intent and meaning of the language employed in the claims." *Bates v. Coe*, 98 U.S. 31, 38 (1878). In addressing the role of the specification, the *Phillips* court quoted with approval its earlier observations from *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998):

> Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.

Phillips, 415 F.3d at 1316. Consequently, *Phillips* emphasized the important role the specification plays in the claim construction process.

The prosecution history also continues to play an important role in claim interpretation. Like the specification, the prosecution history helps to demonstrate how the inventor and the PTO understood the patent. *Id.* at 1317. Because the file history, however, "represents an ongoing negotiation between the PTO and the applicant," it may lack the clarity of the specification and thus be less useful in claim construction proceedings. *Id*. Nevertheless, the prosecution history is intrinsic evidence that is relevant to the determination of how the inventor understood the invention and whether the inventor limited the invention during prosecution by narrowing the scope of the claims. *Id.*

Phillips rejected any claim construction approach that sacrificed the intrinsic record in favor of extrinsic evidence, such as dictionary definitions or expert testimony. The *en banc* court condemned the suggestion made by *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002), that a court should discern the ordinary meaning of the claim terms (through dictionaries or otherwise) before resorting to the specification for certain limited purposes. *Phillips*, 415 F.3d at 1319-24. The approach suggested by *Texas Digital*—the assignment of a limited role to the specification—was rejected as inconsistent with decisions holding the specification to be the best guide to the meaning of a disputed term. *Id*. at 1320-21. According to *Phillips*, reliance on dictionary definitions at the expense of the specification had the effect of "focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of claim terms within the context of the patent." *Id*. at 1321. *Phillips* emphasized that the patent system is based on the proposition that the claims cover only the invented subject matter. *Id.* What is described in the claims flows from the statutory requirement imposed on the patentee to describe and particularly claim what he or she has invented. *Id*. The definitions found in dictionaries, however, often flow from the editors' objective of assembling all of the possible definitions for a word. *Id*. at 1321-22.

Phillips does not preclude all uses of dictionaries in claim construction proceedings. Instead, the court assigned dictionaries a role subordinate to the intrinsic record. In doing so, the court emphasized that claim construction issues are not resolved by any magic formula. The court did not impose any particular sequence of steps for a court to follow when it considers disputed claim language. *Id*. at 1323-25. Rather, *Phillips* held that a court must attach the appropriate weight to the intrinsic sources offered in support of a proposed claim construction,

bearing in mind the general rule that the claims measure the scope of the patent grant. Having read the parties' briefs and carefully considered their arguments and the relevant legal authority, the Court rules as follows:

IV. AGREED CONSTRUCTIONS

Based upon the joint submission of claim construction charts and subsequent arguments in briefing and at the hearing, the following terms of the patent have been agreed to by the parties.

1. "Bus system"

Claim language	Agreed Construction
"Bus system"	"A system used to communicate information according to a bus protocol"

The phrase "bus system" is used in claims 1-5, 17, and 30 of the '181patent; claim 1 of the '077 patent; claims 2-4, 8, and 13 of the '106 patent; claims 4, 7, 8, and 12 of the '871 patent; and claims 15, 18, 21, and 22 of the '998 patent. The phrase is not explicitly defined in the glossary provided in the specifications of the '181 patent, the '077 patent, the '106 patent, or the '871 patent. The specifications of the '181, '077, and '106 patents—the patents relating to the universal bus system—do provide explicit definitions for "E-BUS," "E-BUS MASTER ," "E-BUS SLAVE," "I-BUSn," "II-BUSn," and "IO-BUSn." These definitions are generally directed to a specific type of bus and they do not contradict the proposed construction for the phrase "bus system." For example, the specifications define an "E-BUS" as an external bus outside a unit and an "I-BUS" as an internal bus system of a unit. *See, e.g.,* '181 Patent, 10:53-11:18. Thus, adopting the parties' agreed construction will not contradict a definition provided in the specification. A review of the intrinsic evidence leads the Court to conclude that the parties'

agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

2. "Cell(s)"

Claim language	Agreed Construction
"Cell(s)"	"Configurable element(s)"

The term "cells" is used in claims 6, 8, 10, 23, 31, and 48-49 of the '795 patent; and claims 15, 18, 21, and 22 of the '998 patent. The term is not explicitly defined in the glossary provided in the specifications of the '795 patent or the '998 patent. However, the glossary included in the '520 patent specification does explicitly define "cells" as a "synonym for configurable elements." '520 patent, 6:60. Thus, the parties' agreed construction is consistent with this definition. In addition, the parties have agreed to a construction of the phrase "configurable elements" that is consistent with the definition provided in the specifications of the patents-in-suit. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the term. Therefore, the Court adopts the parties' agreed construction.

3. "Central logic"

Claim language	Agreed Construction
"Central logic"	"A circuit that manages the reconfiguration for all the functional elements"

The phrase "central logic" is used in claims 1 and 11 of the '107 patent. The phrase is not explicitly defined in the glossary provided in the specification of the '107 patent. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the term. Therefore, the Court adopts the

parties' agreed construction.

4. "Communication"

Claim language	Agreed Construction
"Communication"	"Exchange of information"

The term "communication" is used in claims 1, 2, 3-5, 17, and 30 of the '181 patent; claim 1 of the '107 patent; and claim 1 of the '087 patent. The term is not explicitly defined in the glossary provided in the specifications of the '181 patent, the '107 patent, or the '087 patent. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the term. Therefore, the Court adopts the parties' agreed construction.

5. "Configurable element"

Claim language	Agreed Construction
"Configurable element"	"A component of a logic unit, which can be set for a special function by a configuration string/word"

The phrase "configurable element" is used in claims 6, 8, 10, 23, 31, and 48-49 of the '795 patent; and claims 15, 18, 21, and 22 of the '998 patent. The glossary in the '795 patent explicitly defines "configurable element" as "a component of a logic unit, which can be set for a special function using a *configuration string*. Configurable elements are therefore all types of RAM cells, multiplexers, arithmetic logic units, registers, and all types of internal and external interconnecting units, etc." '795 patent, 14:59-66 (emphasis added). The glossary in the '998 patent explicitly defines "configurable element" as "a unit of a logic module which can be set for a special function by a *configuration word*. Configurable elements are thus all types of RAM

cells, multiplexers, arithmetic logic units, registers and all types of internal and external network writing, etc." '998 patent, 13:19-23 (emphasis added). The Court finds that the parties' agreed construction is consistent with the definitions provided in the specifications. Specifically, the '795 patent refers to a "configuration string" and the '998 patent refers to a "configuration word." The parties' agreed construction includes both phrases.

The Court also notes that the parties did not include the second sentence of the definition provided in the specification, which list examples of configurable elements. Thus, it appears that the parties agree that the construction of a term or phrase may require only a part of the explicit definition provided in the specification and need not include the entire definition provided in the specification. Notwithstanding, a review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

6. "Configuration string"

Claim language	Agreed Construction
"Configuration string"	"A series of bits of any length that represents a valid setting for the element to be configured, so that an operable unit is obtained"

The phrase "configuration string" is used in claims 6, 8, 10, 23, 31, and 49 of the '795 patent. The glossary in the '795 patent explicitly defines "configuration string" as "a series of bits, of any length. This bit series represents a valid setting for the element to be configured, so that an operable unit is obtained." '795 patent, 15:11-14. The parties' agreed construction is consistent with the definition provided in the specification. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill

in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

7. "Configuration word"

Claim language	Agreed Construction
"Configuration word"	"A series of bits that are operated on as a unit and represent a valid setting for the element to be configured, so that an operable unit is obtained"

The phrase "configuration word" is used in claims 1 and 11 of the '107 patent; and claim 15 of the '869 patent. The phrase is not explicitly defined in the glossary of the '107 patent and the '869 patent does not include a glossary. However, the glossary included in the '998 patent specification does explicitly define "configuration word" as "a bit series of any desired length. This bit series represents a valid setting for the element to be configured, so that a functional unit is obtained." '998 Patent, 13:30-33. The Court finds that the parties' agreed construction is consistent with the definition provided in the specification of the '998 patent. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

8. "DFP"

Claim language	Court Construction
"DFP"	"Data flow processor according to German Patent DE 44 16 881"

The term "DFP" is used in claim 1 of the '077 patent and claims 2-4, 8, and 13 of the '106 patent. The glossary in the '077 patent and the '106 patent explicitly define "DFP" as

"Data flow processor according to German Patent DE 44 16 881." *See, e.g.*, '077 patent, 14:17-18. The Court finds that the parties' agreed construction is consistent with the definition provided in the specification. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the term. Therefore, the Court adopts the parties' agreed construction.

9. "DPGA"

Claim language	Agreed Construction
"DPGA"	"Dynamically programmable gate array"

The term "DPGA" is used in claim 1 of the '077 patent and claims 2-4, 8, and 13 of the '106 patent. The glossary in the '077 patent and the '106 patent explicitly define "DPGA" as "Dynamically programmable gate array. Related art." *See, e.g.,* '077 patent, 14:19-21. The Court finds that the parties' agreed construction is consistent with the definition provided in the specification. The Court notes that the parties did not include the second sentence of the definition provided in the specification, which states "[r]elated art." As before, it appears that the parties agree that the construction of a term or phrase may only require part of the explicit definition provided in the specification and need not include the entire definition provided in the specification. Notwithstanding, a review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the term. Therefore, the Court adopts the parties' agreed construction.

10. "Functional element"

Claim language	Agreed Construction
"Functional element"	"An individual configurable element or group of configurable elements that performs a function"

The phrase "functional element" is used in claims 1 and 11 of the '107 patent. The phrase is not explicitly defined in the glossary provided in the specification of the '107 patent. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

11. "FPGA"

Claim language	Agreed Construction
"FPGA"	"Field programmable gate array"

The term "FPGA" is used in claim 1 of the '077 patent and claims 2-4, 8, and 13 of the '106 patent. The glossary in the '077 patent and the '106 patent explicitly define "FPGA" as "Field programmable gate array. Related art." *See, e.g.*, '077 patent, 14:42. Thus, the parties' agreed construction is consistent with the definition provided in the specification. The Court notes that the parties did not include the second sentence of the definition provided in the specification, which states "[r]elated art." Additionally, the glossary in the specification of the '871 patent defines "FPGA" as "[k]nown field-programmable gate array." Notwithstanding, a review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the term. Therefore, the Court adopts the parties' agreed construction.

12. "Grouping"/ "grouped"

Claim language	Agreed Construction
"Grouping"	"Forming into a collection of objects considered together"
"Grouped"	"Having formed into a collection of objects considered together"

The terms "grouping" and "grouped" are used in claims 1, 15, 16, and 18 of the '242 patent; and claims 55, and 56 of the '869 patent. The specifications of the '242 patent and the '869 patent do not include a glossary of terms like the other patents-in-suit. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the terms. Therefore, the Court adopts the parties' agreed construction.

13. "Higher-level unit"

Claim language	Agreed Construction
"Higher-level unit"	"A supervisory unit"

The phrase "higher-level unit" is used in claims 1 and 11 of the '107 patent. The phrase is not explicitly defined in the glossary provided in the specification of the '107 patent. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the claim term. Therefore, the Court adopts the parties' agreed construction.

14. "Interface"

Claim language	Agreed Construction
"Interface"	"Unit providing permanent implementation of a bus system control for communicating information across a shared boundary"

The term "interface" is used in claims 2, 3, and 8 of the '106 patent. The term is not explicitly defined in the glossary provided in the specification of the '106 patent. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the term. Therefore, the Court adopts the parties' agreed construction.

15. "Interface unit"

Claim language	Agreed Construction
"Interface unit"	"Unit providing permanent implementation of a bus system control for communicating information across a shared boundary"

The phrase "interface unit" is used in claims 1, 2, 3-5, 17, and 30 of the '181 patent. The phrase is not explicitly defined in the glossary provided in the specification of the '181 patent. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

16. "State machine for controlling the at least one interface unit"

Claim language	Agreed Construction
"State machine for controlling the at least one interface unit"	"Permanent, predefined state machine for controlling the interface unit"

The phrase "state machine for controlling the at least one interface unit" is used in claims 1 and 2 of the '181 patent. The phrase "state machine" is a disputed term that will be discussed in more detail below, while the construction of the phrase "interface unit" was agreed to by the parties and adopted by the Court. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

17. "State machine controls the at least one interface"

Claim language	Agreed Construction
"State machine controls the at least one interface"	"Permanent, predefined state machine that controls an interface"

The phrase "state machine controls the at least one interface" is used in claim 3 of the '106 patent. The phrase "state machine" is a disputed term that will be discussed in more detail below, while the construction of the phrase "interface" was agreed to by the parties and adopted by the Court. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

18. "State machine controls an external bus"

Claim language	Agreed Construction
"State machine controls an external bus"	"Permanent, predefined state machine that controls an external bus"

The phrase "state machine controls an external bus" is used in claim 4 of the '106 patent and claim 2 of the '181 patent. The phrase "state machine" is a disputed term that will be discussed in more detail below. A review of the intrinsic evidence leads the Court to conclude

that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

19. "Synchronization signal"

Claim language	Agreed Construction
"Synchronization signal"	"A status signal generated by a configurable element or a processor and relayed to other configurable elements or processors that controls and synchronizes data processing"

The phrase "synchronization signal" is used in claims 1, 6, 9, 15, 16, and 18 of the '242 patent; claim 17 of the '869 patent; and claims 15, 18, 21, 22 of the '998 patent. The glossary in the '998 patent explicitly defines "synchronization signals" as "status signals generated by a configurable element or a processor and relayed to other configurable elements or processors to control and synchronize the data processing. It is also possible to return a synchronization signal with a time lag (stored) to one and the same configurable element or processor." '998 patent, 13:66-14:4. The Court finds that the parties' agreed construction is consistent with the definition provided in the specification. The Court also notes that the parties did not include the second sentence of the definition provided in the specification. As before, it appears that the parties agree that the construction of a term or phrase may require only a part of the explicit definition provided in the specification and need not include the entire definition provided in the specification. Notwithstanding, a review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

20. "Synchronizing data processing"

Claim language	Agreed Construction
"Synchronizing data processing"	"Coordinating the relative timing of two or more data processing events"

The phrase "synchronizing data processing" is used in claims 1, 5, 6, 9, 15, 16, and 18 of the '242 patent; and claims 15, 18, 21, and 22 of the '998 patent. The phrase is not explicitly defined in the glossary provided in the specification of the '998 patent and the specification of the '242 patent does not include a glossary. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

21. "The plurality of synchronization signals"

Claim language	Agreed Construction
"The plurality of synchronization signals"	"Two or more synchronization signals"

The phrase "the plurality of synchronization signals" is used in claim 17 of the '869 patent. The construction of the phrase "synchronization signals" was agreed to by the parties and the parties' proposed construction of this phrase denotes that a plurality is two or more. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

22. "Without effecting other processing array elements and without effecting data streams communicated between transmitters and receivers"

Claim language	Agreed Construction
"Without effecting other processing array elements and without effecting data streams communicated between transmitters and receivers"	"Without affecting other processing array elements and without affecting data streams communicated between transmitters and receivers"

This phrase is used in claim 4 of the '871 patent. The parties' proposed construction substitutes "affecting" for "effecting" in the phrase. A review of the intrinsic evidence leads the Court to conclude that the parties' agreed construction is how a person of ordinary skill in the art would interpret the phrase. Therefore, the Court adopts the parties' agreed construction.

V. TERMS IN DISPUTE OF THE PATENTS-IN-SUIT

The parties have identified nineteen groups of disputed terms or phrases, with a number of these groups consisting of multiple terms.

1. "Configure/Reconfigure Terms"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Configure"	Set the function and interconnection of a logic unit, a FPGA cell, logic cell, or a PAE	Set the function and interconnection of a logic unit, a FPGA cell, logic cell or a PAE (see reconfigure)
Court's Construction	Set the function and interconnection of a logic unit, a FPGA cell, logic cell, or a PAE	
"Configuring"	Setting the function and interconnection of a logic unit, a FPGA cell, logic cell, or a PAE	Setting the function and interconnection of a logic unit, a FPGA cell, logic cell or a PAE (see reconfigure)
Court's Construction	Setting the function and interconnection of a logic unit, a FPGA cell, logic cell, or a PAE	

"Configured"	Having set the function and interconnection of a logic unit, a FPGA cell, logic cell, or a PAE	Having set the function and interconnection of a logic unit, a FPGA cell, logic cell or a PAE (see reconfigure)
Court's Construction	Having set the function and interconnection of a logic unit, a FPGA cell, logic cell, or a PAE	
"Configurable"	Capable of being configured	Capable of having the function and interconnection of a logic unit, a FPGA cell, logic cell or a PAE set (see reconfigure)
Court's Construction	Capable of having the function and interconnection of a logic unit, a FPGA cell, logic cell, or a PAE set	
"Reconfigure(s)"	Reset(s) with a new configuration while any remaining logic units, FPGA cells, logic cells or PAEs that do not participate in the reconfiguration continue with their same functions"	New configuration of any number of PAEs or logic cells, while any remaining PAEs or logic cells continue with the same function (see configure)
Court's Construction	Reset(s) any number of logic units, FPGA cells, logic cells or PAEs with a new configuration, while any remaining logic units, FPGA cells, logic cells, or PAEs continue with the same function	
"Reconfiguring"	Resetting with a new configuration while any remaining logic units, FPGA cells, logic cells or PAEs that do not participate in the reconfiguration continue with their same functions"	New configuration of any number of PAEs or logic cells, while any remaining PAEs or logic cells continue with the same function (see configure)
Court's Construction	Resetting any number of logic units, FPGA cells, logic cells, or PAEs with a new configuration, while any remaining logic units, FPGA cells, logic cells, or PAEs continue with the same function	
"Reconfigured"	Having reset with a new configuration while any remaining logic units, FPGA cells, logic cells or PAEs that do not participate in the reconfiguration continue with their same functions"	New configuration of any number of PAEs or logic cells, while any remaining PAEs or logic cells continue with the same function (see configure)
Court's Construction	Having reset any number of logic units, FPGA cells, logic cells, or PAEs with a new configuration, while any remaining logic units, FPGA cells, logic cells, or PAEs continue with the same function	

"Perform reconfiguration"	Reconfigure	Perform a new configuration of any number of PAEs or logic cells while any remaining PAEs or logic cells continue with the same function (see configure)"
Court's Construction	Perform a new configuration of any number of logic units, FPGA cells, logic cells, or PAEs, while any remaining logic units, FPGA cells, logic cells, or PAEs continue with the same function	
"Reconfigurable"	Capable of being reconfigured	Capable of having a new configuration of any number of PAEs or logic cells while any remaining PAEs or logic cells continue with the same function (see configure)
Court's Construction	Capable of resetting any number of logic units, FPGA cells, logic cells, or PAEs with a new configuration, while any remaining logic units, FPGA cells, logic cells, or PAEs continue with the same function	
"Reconfiguration" (n.)	A new configuration that is undertaken while any remaining logic units, FPGA cells, logic cells or PAEs that do not participate in the reconfiguration continue with their same functions	New configuration of any number of PAEs or logic cells while any remaining PAEs or logic cells continue with the same function (see configure)
Court's Construction	New configuration of any number of logic units, FPGA cells, logic cells, or PAEs while any remaining logic units, FPGA cells, logic cells, or PAEs continue with the same function	
"Configuration" (n.)	the function and interconnection of a logic unit, a FPGA cell, logic cell, or a PAE	the function and interconnection of a logic unit, a FGPA cell, logic cell or PAE (see reconfigure)
Court's Construction	The function and interconnection of a logic unit, a FPGA cell, logic cell, or a PAE	

The Court construes each of the disputed phrases as indicated in the table above.

A. Parties' Construction Arguments

In general, the parties' proposed constructions are very close to the explicit definitions provided in the specification. The parties' main dispute is whether the constructions should

include the additional parenthetical "(see reconfigure)" and "(see configure)."[1] Defendants contend that the parenthetical should be included because it provides context for the terms and confirm the terms are related. Plaintiff argues that including the parenthetical will only confuse the jury.

B. Analysis

To begin its analysis, the Court first turns to the language of the claims, as it provides "substantial guidance as to the meaning of particular claim terms." *Phillips*, 415 F.3d at 1313 (citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). The terms "configure," "configuring," and "configured" appear in claims 1, 5, 9, and 16 of the '242 patent; claims 13, 14, 15, 17, 18, 19, and 65 of the '869 patent; claim 1 of '087 patent; claim 30 of the '181 patent; claims 7, 11, and 12 of the '520 patent; and claim 7 of the '871 patent. The term "configurable" appears in claims claim 7 of the '871 patent; claim 1 of the '087 patent; claims 6, 8, 10, 23, 48, and 49 of the '795 patent; and claims 15, 18, 21, and 22 of the '998 patent. The term "configuration" appears in claims 8 and 10 of the '795 patent; claim 5 of the '242 patent; and claim 1 of the '087 patent. The terms "reconfigure(s)," "reconfiguring," and "reconfigured" appear in claims 1, 5, 6, 9, 15, 16, 18, and 23 of the '242 patent; claims 13, 18, 19, 56, and 65 of the '869 patent; and claims 6, 8, 23, 31, 48, and 49 of the '795 patent. The term "perform reconfiguration" appears in claims 1 and 11 of the '107 patent. The term "reconfigurable" appears in claims 4, 7, 8, and 12 of the '871 patent; claim 1 of the '087 patent; claim 17 of the

[1] In its Surreply Brief, Defendants note that they are amenable to modifying their proposed construction of "reconfigure" to avoid defining a verb with the noun "configuration." Dkt. No. 148 at 4. The Court therefore adopts Plaintiff's proposal of using "reset" for these terms.

‘181 patent; claim 6 of the ‘795 patent; and claim 11 of the ‘107 patent. The term “reconfiguration” appears in claim 1 of the ‘087 patent.

Two things are evident from the claim language. First, the phrases are used consistently in each patent and are meant to have the same meaning in the claims and the patents in which they are used. This is not disputed, as evidenced by the parties’ proposed constructions. Second, the terms are not explicitly defined in the claims. Thus, the Court next turns to the specification as it “is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.” *Id.* at 1315 (citation omitted).

The specifications of the ‘871 Patent, ‘087 Patent, ‘181 Patent, ‘795 Patent, ‘998 Patent, and ‘520 Patent each provide an explicit definition for “configure,” “reconfigure,” or a variation thereof. *Martek Biosciences Corp. v. Nutrinova, Inc.*, 579 F.3d 1363, 1380 (Fed. Cir. 2009) (“When a patentee explicitly defines a claim term in the patent specification, the patentee's definition controls.”). The Court notes that even though there are some minor differences between the definitions provided in the specifications, theses differences are not substantive. In general, the specifications define “configure” as “[s]etting the function and interconnections of a logic unit, an FPGA cell or a PAE (see reconfigure)” and “reconfigure” as “[n]ew configuration of any number of PAEs, while any remaining number of PAEs continue their functions (see configure).” *See, e.g,* ‘795 patent, 15:1-65. Because the patentee has chosen to be his own lexicographer, the Court’s construction follows the explicit definitions provided in the specifications. *Vitrionics,* 90 F.3d at 1582 (“The specification acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication.”). The Court further finds that these explicit definitions do not contradict the claim language. This is true for

all of the patents-in-suit, even the '242 patent and '869 patent, which does not include a glossary in the specification.

In addition, the Court concludes that including the parenthetical, as proposed by Defendants, is not necessary and will only confuse the jury. Specifically, the use of the terms in the claims and the Court's construction indicate that these terms are related without the risk of juror confusion. For example, the Court construes "configure" as "set the function and interconnection of a logic unit, a FPGA cell, logic cell, or a PAE" and "reconfigure" as "reset any number of logic units, FPGA cells, logic cells or PAEs with a new configuration, while any remaining logic units, FPGA cells, logic cells or PAEs continue with the same function." The relationship of these terms are even more evident when viewed in light of exemplary claim 1 of the '242 patent that recites "at least some of said cells being selectively *configured* to perform a first function, the at least some of said cells being selectively *reconfigured* to perform a second function, the second function being different than the first function." Claim 1 of the '242 patent (emphasis added). The relationship between configuring and reconfiguring is indicated by the claim language itself and need not be included in the Court's construction. Thus, even though the explicit definition provided in the specification includes a parenthetical, the Court believes that including the parenthetical will only confuse the jury. *Funai Elec. Co., Ltd. v. Daewoo Elecs. Corp.*, 616 F.3d 1357, 1366 (Fed. Cir. 2010) ("The criterion is whether the explanation aids the court and the jury in understanding the term as it is used in the claimed invention."). Similarly, as discussed above, the parties obviously agree that the entire definition of the term or phrase provided in the specification is required to properly construe a claim term. For example, the parties' agreed construction for the terms "DPGA" and "FPGA" omits the parenthetical

"(related art)." As with a number of the agreed terms, omitting the parenthetical does not change the explicit definition provided in the specification.

The Court also notes that Plaintiff included a limitation in its proposed construction of the "reconfigure" terms that is not included in the explicit definitions provided in the specifications. For example, Plaintiff's proposed construction for "reconfigure" is "reset with a new configuration while any remaining logic units, FPGA cells, logic cells or PAEs *that do not participate in the reconfiguration* continue with their same functions." The Court finds that none of the explicit definitions provided in the specification includes the "that do not participate in the reconfiguration" language. The Court therefore rejects including this language in the construction, and instead follows the explicit definition provided by the patentee. Accordingly, consistent with their use in the intrinsic evidence, the Court construes the disputed phrases as indicated in the table above.

2. "Arithmetic-Logically Configure/Reconfigure Terms"

Claim Term or Phrase	**PACT's Proposed Construction**	**Xilinx's & Avnet's Proposed Construction**
"Arithmetic-logically configure"	Setting the function and interconnections to perform arithmetic or logical operations.	Setting the function and interconnections to perform arithmetic and logical operations. Using multiplexers to select inputs to an ALU or registers is not sufficient to arithmetic-logically configure.

"Arithmetic-logically reconfigure"	Changing the function and/or interconnections to perform different arithmetic and logical operations	Changing the function and interconnections to perform different arithmetic and logical operations. Using multiplexers to select inputs to an ALU or registers; operating in different modes, such as operating in SIMD or MIMD mode; or switching inputs of a cell directly to the cell output is insufficient to arithmetic logically reconfigure

The Court construes "arithmetic-logically configure" as "set the function and interconnection of a cell to perform arithmetic and logical operations," and "arithmetic-logically reconfigure" as "reset any number cells with a new function and interconnection to perform arithmetic and logical operations, while any remaining cells continue with the same function."

A. Parties' Construction Arguments

The parties dispute: (1) whether arithmetic-logically configuring and reconfiguring can be met by performing an arithmetic or logical operation alone; (2) whether both "function and interconnection" need to change to "arithmetic-logically reconfigure;" and (3) whether statements in the file history disclaiming "using multiplexers to select inputs to an ALU or registers," "operating in different modes, such as operating in SIMD or MIMD mode," and "switching inputs of a cell directly to the cell output" should limit the claim terms. During the claim construction hearing Plaintiff provided a compromise construction that is presented in the table above.

B. Analysis

To begin its analysis, the Court first turns to the language of the claims. The disputed phrases appear in claims 13, 14, 15, 17, 18, and 19 of the '869 patent. Independent claims 13 of the '869 patent recites:

> 13. A massively parallel data processing apparatus comprising:
> a plurality of computing cells arranged in a multidimensional matrix, the plurality of computing cells capable of simultaneously manipulating a plurality of data, each of the plurality of computing cells including:
> an input interface for receiving a plurality of input signals,
> a plurality of logic members, at least one of the plurality of logic members coupled to the input interface,
> at least one coupling unit selectively coupling at least one of the plurality of logic members to another of the plurality of logic members a function of at least one of a plurality of configuration signals to ***arithmetic-lopically*** [sic] configure the computing cell prior to processing the input signals, wherein coupled logic members perform at least one select ***arithmetic-logic*** operation on the input signals to process the input signals, the at least one select ***arithmetic-logic*** operation being dependent on the at least one of the plurality of configuration signals,
> a register unit selectively storing a portion of the processed input signals, and
> an output interface for transmitting the processed input signals, wherein the input interface of at least one of the plurality of computing cells is selectively coupled to the output interface of at least another of the plurality of computing cells;
> a configuration interface for transmitting the plurality of configuration signals to at least some of the plurality of computing cells to ***arithmetic-logically configure*** and ***arithmetic-logically reconfigure*** the at least some of the plurality of computing cells; and
> a configuration unit coupled to the configuration interface, the configuration unit generating the plurality of configuration signals, the at least some of the plurality of computing cells being configured as a function of the at least one configuration signal during operation of the massively parallel data processing apparatus such that others of the plurality of computing cells not being configured are not haltered or impaired in their operations. (emphasis added)

Claim 13 recites three main elements of the data processing apparatus: (1) a plurality of computing cells; (2) a configuration interface; and (3) a configuration unit. The plurality of computing cells are arranged in a multidimensional matrix and are capable of simultaneously manipulating a plurality of data. Each of the computing cells includes at least five elements: (1) an input interface; (2) a plurality of logic members; (3) at least one coupling unit; (4) a register unit, and (5) an output interface. Moreover, each of the computing cells receives two different signals, a configuration signal and an input signal. Based on the first signal it receives—the configuration signal—the coupling unit couples the logic members of the computing cells in preparation to perform an *arithmetic-logic* operation on the second signal it receives—the input signal. As recited in the claims, this coupling is done prior to processing the input signal. Once the logic coupling is complete, the "coupled logic members perform at least one select *arithmetic-logic* operation on the input signals [the second signal] to process the input signals, the at least one select *arithmetic-logic* operation being dependent on the at least one of the plurality of configuration signals." Thus, the claims indicate that the computing cell is configured to perform an arithmetic-logic operation on the input signal. And as indicated by the intrinsic evidence, an arithmetic-logic operation includes one of the four basic arithmetic operations (*i.e.*, addition, subtraction, multiplication, and division). '869 Patent, 4:58-5:20; 6:52-9:59; Figs. 4, 11, and 18. Thus, plaintiff's assertion that an "arithmetic-logically configure/reconfigure**"** can include only a logical operation is not supported by the intrinsic evidence.

Instead, "arithmetic-logically configure/reconfigure" requires a configuration that is capable of performing an arithmetic operation on the input signal, which inherently also includes

performing a logic operation on the input signal because the arithmetic operation is executed with logic members. Indeed, the specification states:

> The *core of the present invention* consists in proposing a data flow processor of cellular structure whose cells allows reconfiguration in an arithmetic-logical sense, quasi randomly, via an external loading logic. *Of extreme necessity* is that the respective cells allow reconfiguration individually and without affecting the remaining cells or disabling the entire module. *Thus*, the data flow processor *according to the present invention* can be "programmed" as an adder in a first operating cycle and as a multiplier in a subsequent operating cycle, wherein the number of cells required for addition or multiplication may well be different and the placement of already loaded MACROs is upheld.

'869 Patent, 2:19-31 (emphasis added). As indicated by the specification, the "core of the present invention" is for the claimed computing cells to perform arithmetic-logic operation, which necessarily includes arithmetic operations (*e.g.*, addition or multiplication) based on coupling logic members of the computing cells. To be sure, the function and interconnection of these computing cells is distinguished from the function and interconnection of other logic cells included in the DFP that "are loaded prior to loading the programs and remain constant usually for the entire run time" to ensure that the data flow processor (DFP) can adapt to its hardware environs. '869 Patent, 2:46-51. Simply stated, the recited computing cells are "arithmetic-logically configured/reconfigured" to perform the arithmetic operations on the recited input signal. Plaintiff's proposed construction is broader than what is claimed because any logic operation (AND, OR, or XOR) would satisfy the claim limitation. This would effectively read "arithmetic" out of the recited claims. The intrinsic evidence does not support such a construction, but instead requires that the computing cells to be "arithmetic-logically configured/reconfigured" to perform an arithmetic and logical operation.

Plaintiff argues that such a construction would exclude the "preferred embodiment" disclosed in Figure 12 of the '869 Patent. The Court disagrees. As indicated by the specification, Figure 12 is a simple example of a cell structure. Moreover, the figure illustrates what is explicitly recited in the claims prior to performing an arithmetic-logic operation on an input signal. That is, the figure provides an example of "selectively coupling at least one of the plurality of logic members [*e.g.,* AND member 51] to another of the plurality of logic members [e.g. XOR member 53]" as a function of the configuration signal provided by complier 30. '869 Patent, 9:50-10:19. Again, the claims recite that this coupling is prior to performing the arithmetic-logic operation on the input signal. After the logic members are coupled, the "coupled logic members perform at least one select *arithmetic-logic* operation on the input signals to process the input signals." The Court's construction does not exclude this embodiment because the coupling of logical members illustrated in Fig. 12 is explicitly recited in the claims. Plaintiff's proposed construction, however, improperly asks the Court to construe the "arithmetic-logically configured/reconfigure" to stop at the logical coupling and ignore the remaining claim language.

The next dispute relating to these phrases is Defendants' inclusion of a negative limitation in their proposed construction for "arithmetic-logically configure/reconfigure." Specifically, Defendants proposed construction states that "[u]sing multiplexers to select inputs to an ALU or registers is not sufficient to arithmetic-logically configure." Defendants contend that the patentee disclaimed using multiplexers for "arithmetic-logical" configuration in the prosecution history. The Court has reviewed the intrinsic evidence and concludes that including this negative limitation is not required and will only confuse the jury. In distinguishing the invention, the patentee argued that using multiplexer to select inputs to an ALU and PME

register is not arithmetic-logically configure or reconfigure. (Dkt. No. 142-7 at 164.) The patentee also argued that changing the PME to operate in SIMD or in MIMD mode is not an arithmetic-logic reconfiguration**.** (Dkt. No. 142-7 at 165-166.) The Court concludes that the patentee's statements are not a clear disavowal of claim scope. Instead, the statements confirm what appears to be readily apparent to a person of ordinary skill in the art that merely selecting an input to an ALU or changing the operation mode of a PME from SIMD to MIMD by itself does not constitute arithmetic-logically configuring or reconfiguring a computing cell. Indeed, this was confirmed by Plaintiff's expert, Dr. Tredennick, when he stated that "it would be readily apparent to persons of ordinary skill that changing the cell from SIMD to MIMD mode is neither arithmetic-logic configuration nor arithmetic-logic reconfiguration." (Dkt. No. 142-76 at ¶ 39.) Thus, the Court believes that including this negative limitation is not necessary and will only confuse the jury. More importantly, the Court's construction requires setting or resetting the cell to perform arithmetic and logical operations in order for the computing cell to be arithmetic-logically configured/reconfigure, and not merely selecting an input to an ALU.

The final dispute relating to the phrase "arithmetic-logically configured/reconfigure" is whether both "function and interconnection" need to change to "arithmetic-logically configure/reconfigure." The Court addressed this argument with regard to disputed terms "configure" and "reconfigure." As discussed above, the term "configure" and "reconfigure" is explicitly defined in the specification of the '520 patent and '720 patent. Furthermore, the parties did not argue that the terms "configure" and "reconfigure" should be construed differently for each patent. Instead, the parties provided only one construction for these terms as they apply to all of the asserted claims. Therefore, the Court's construction as it relates to the

"configure" and "reconfigure" forms the basis for its construction of the disputed phrases "arithmetic-logically configure/reconfigure." For the reasons stated above, and based on the explicit definitions provided by the patentee for "configuration," the Court construes "arithmetic-logically configure" to mean "set the function and interconnection of a cell to perform arithmetic and logical operation." Similarly, based on the explicit definitions provided by the patentee for "reconfiguration," the Court construes "arithmetic-logically reconfigure" to mean "reset any number cells with a new function and interconnection to perform arithmetic and logical operations, while any remaining cells continue with the same function."

3. "Dynamically Reconfigure Terms"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Dynamically reconfigure"	Reset with a new configuration while any remaining ones that do not participate in the reconfiguration continue processing data according to their same functions"	See Defendants' construction of "reconfigure" above. The term "dynamically" should be given its plain meaning to one of ordinary skill in the art.
Court's Construction	Halt and reset any number of logic units, FPGA cells, logic cells or PAEs with a new configuration, while any remaining logic units, FPGA cells, logic cells or PAEs continue with the same function	
"Dynamically reconfiguring"	Resetting with a new configuration while any remaining ones that do not participate in the reconfiguration continue processing data according to their same functions	See Defendants' construction of "reconfigure" above. The term "dynamically" should be given its plain meaning to one of ordinary skill in the art.
Court's Construction	Halting and resetting any number of logic units, FPGA cells, logic cells or PAEs with a new configuration, while any remaining logic units, FPGA cells, logic cells or PAEs continue with the same function	
"Dynamically reconfigurable module"	A module with functional elements that can be reset with a new configuration while any remaining ones that do not participate in the reconfiguration continue processing data according to their same functions"	See Defendants' construction of "reconfigurable" above. The term "dynamically" should be given its plain meaning to one of ordinary skill in the art.
Court's Construction	A module capable of halting and resetting any number of functional elements with a new configuration, while any remaining functional elements continue with the same function	
"Dynamically reconfigurable cells"	Cells that can be reset with a new configuration while any remaining ones that do not participate in the reconfiguration continue processing data according to their same functions	See Defendants' construction of "reconfigurable" and "cell" above. The term "dynamically" should be given its plain meaning to one of ordinary skill in the art.
Court's Construction	A cell that can be halted and reset with a new configuration, while any remaining cells continue with the same function	

The Court construes each of the disputed phrases as indicated in the table above.

A. Parties' Construction Arguments

The dispute is whether the Court should construe "dynamically" in the phrase "dynamically reconfigured." Defendants contend that "reconfigure" has already been construed and that the term dynamically should be given its plain and ordinary meaning. Plaintiff proposes a construction for "dynamically reconfigured" that mirrors their proposed construction for "reconfigured."

B. Analysis

To begin its analysis, the Court first turns to the language of the claims. The phrases "dynamically reconfigure" and "dynamically reconfiguring" appear in claims 5, 9, 18, and 19 of the '242 patent; claims 18 and 19 of the '869 patent; and claims 6, 8, 10, 23, 31, 48, and 49 of the '795 patent. The phrase "dynamically reconfigurable module" appears in claim 11 of the '107 patent. The phrase "dynamically reconfigurable cells" appears in claim 17 of the '181 patent. Two things are evident from the claim language. First, the phrases are used consistently in each patent and are meant to have a similar meaning. The parties do not dispute this as evidenced by their proposed constructions. Second, the terms are not explicitly defined in the claims. Thus, the Court turns to the specification.

The specification of the '242 patent states that in the context of reloading a module, "dynamically" means that "only the parts to be reloaded are halted while the rest continues to operate." '242 Patent, 8:58-60. Thus, the term dynamic in this context means that the module's operations are halted before the reconfiguration takes place. Additionally, as discussed above, the Court construes "reconfigure" as "reset(s) any number of logic units, FPGA cells, logic cells,

or PAEs with a new configuration, while any remaining logic units, FPGA cells, logic cells, or PAEs continue with the same function." Given this definition for "reconfigure," the Court concludes that "dynamically reconfigure" means "halt and reset any number of logic units, FPGA cells, logic cells or PAEs with a new configuration, while any remaining logic units, FPGA cells, logic cells or PAEs continue with the same function." This analysis equally applies to the other variations of the "dynamically reconfigure" phrase.

To support its construction, Plaintiff contends that this specification passage provides an explicit definition for "dynamic reconfiguration." '242 patent, 8:56-60 ("since the module is being reloaded dynamically, that is, only the parts to be reloaded are halted while the rest continues to operate."). Defendants correctly argue, however, that Plaintiff's proposed construction deviates from what is disclosed in the specification. Specifically, Plaintiff's construction leaves out the concepts of "reloading" and "halting," and also swaps "continue to process data" for "continues to operate." Thus, Plaintiff's proposed construction is inconsistent with the intrinsic evidence it attempts to rely on. Defendants, however, do not offer a proposed construction for "dynamically." *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351,1362 (Fed. Cir. 2008) ("[W]hen the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it."). Accordingly, for the reasons discussed above, the Court construes each of the disputed phrases as indicated in the table above based on the analysis for the term "reconfigure" and the intrinsic evidence.

4. "Multi-Dimensional Terms"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Cell units arranged as a multi-dimensional array"	The cell units are systematically arranged for interconnection in at least two dimensions"	"an array of cell units disposed such that each cell has connections to adjoining cells in two or more dimensions
Court's Construction	an array of cell units disposed such that each cell has connections in two or more dimensions	
"Cells arranged in a multidimensional matrix"	The cells are systematically arranged for interconnection in at least two dimensions	a matrix of cells disposed such that each cell has connections to adjoining cells in two or more dimensions"
Court's Construction	a matrix of cells disposed such that each cell has connections in at least two dimensions	
"Cells arranged in a Multidimensional pattern"	The cells are systematically arranged for interconnection in at least two dimensions	a pattern of cells disposed such that each cell has connections to adjoining cells in two or more dimensions
Court's Construction	a pattern of cells disposed such that each cell has connections in at least two dimensions	
"Cells arranged in a pattern having two or more dimensions"	The cells are systematically arranged for interconnection in at least two dimensions	a pattern of cells disposed such that each cell is connected to adjoining cells in two or more dimensions
Court's Construction	a pattern of cells disposed such that each cell has connections in at least two dimensions	
"Multidimensional cell arrangement"	The cells are systematically arranged for interconnection in at least two dimensions	an arrangement of cells disposed such that each cell has connections to adjoining cells in two or more dimensions
Court's Construction	an arrangement of cells disposed such that each cell has connections in at least two dimensions	
"Cells arranged in a pattern having at least two dimensions"	Cells that are systematically arranged for interconnection in at least two dimensions	a pattern of cells disposed such that each cell is connected to adjoining cells in two or more dimensions
Court's Construction	a pattern of cells disposed such that each cell has connections in at least two dimensions	

"Multi-dimensional programmable cell architecture"	Fundamentally having programmable cells that are systematically arranged for interconnection in at least two dimensions	cell architecture disposed such that each programmable cell has connections to adjoining programmable cells in two or more dimensions
Court's Construction	a pattern of programmable cells disposed such that each cell has connections in at least two dimensions	

The Court construes each of the disputed phrases as indicated in the table above.

A. Parties' Construction Arguments

The parties agree that this phrase requires connections or interconnection in at least two dimensions. What the parties disagree on is: (1) whether the cells in the multidimensional array, pattern, matrix, architecture, etc. are laid out so that adjoining cells are connected to one another in a two dimensional pattern, as Defendants contend; and (2) whether the term "architecture" should be construed to mean "fundamentally" having programmable cells arranged in a particular way, as Plaintiff contends.

B. Analysis

To begin its analysis, the Court first turns to the language of the claims. The phrase "cell units arranged as a multi-dimensional array" appears in claim 1 of the '087 patent. The phrase "cells arranged in a multidimensional matrix" appears in claims 13, 14, 15, 18, and 19 of the '869 patent. The phrase "cells arranged in a multidimensional pattern" appears in claim 65 of the '869 patent; and claims 7, 11, and 12 of the '520 patent. The phrase "cells arranged in a pattern having two or more dimensions" appears in claims 1, 6, and 9 of the '242 patent. The phrase "multidimensional cell arrangement" appears in claims 8, 10, 23, 31, and 49 of the '795 patent. The phrase "cells arranged in a pattern having at least two dimensions" appears in claim 15 of the '242 patent. The phrase "multi-dimensional programmable cell architecture" appears

in claims 1, 2, 3, 4, 17, and 30 of the '181 patent; claims 2-4, 8, and13 of the '106 patent; and claim 1 of the '077 patent.

With respect to the first dispute, the Court concludes that there is nothing in the claim language or intrinsic evidence requiring each cell to be connected to an adjoining cell in two or more dimensions. For example, claim 1 of the '087 patent recites "a plurality of addressable configurable cell units arranged as a multidimensional array, interconnected by the plurality of data buses." To illustrate this limitation, Figure 1 and 3 of the '181 patent, Figure 6 of the '242 patent, and Figure 1 of the '871 patent provide examples where the cell units are connected to data buses, and not just to an adjoining cells. Thus, Defendants' proposed construction attempts to import limitations from some of the preferred embodiments into the claims. As indicated by the identified figures, the interconnection of the cells does not have to be to adjoining cells. Thus, the Court rejects this portion of Defendants' proposed construction.

Regarding the second dispute, Defendants argue that the term "architecture" is commonly understood and does not need to be construed. Plaintiff contends that jury will confuse the term "architecture" with building architecture. Thus, Plaintiff's proposed construction includes "fundamentally having programmable cells that are systematically arranged for interconnection in at least two dimensions." The Court finds that the term "fundamentally" in Plaintiff's proposed construction is not supported by the intrinsic evidence. Moreover, the Court agrees that including the term "fundamentally" only adds ambiguity to the construction and would not help clarify the disputed term for the jury. Therefore, the Court construes "multi-dimensional programmable cell architecture" to mean "a pattern of programmable cells disposed such that each cell has connections in at least two dimensions."

5. "Register Terms and Configuration Memory"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
Command register	Dedicated register that stores the function for the configurable element"	The function to be carried out by the configurable element is entered in this register.
Court's Construction	The function to be carried out by the configurable element is entered in this register.	
Configuration register	Dedicated register that stores the configuration information of a cell"	Register that stores the configuration information of a cell
Court's Construction	Register that stores the configuration information of a cell	
Configuration Memory	A storage device that contains only one or more configuration strings"	The configuration memory contains one or more configuration strings"
Court's Construction	The configuration memory contains one or more configuration strings	

The Court construes each of the disputed phrases as indicated in the table above.

To begin its analysis, the Court first turns to the language of the claims. The phrase "command register" appears in claims 11 and 12 of the '520 patent. The phrase "configuration register" appears in claims 7, 11, and 12 of the '520 patent; and claim 22 of the '998 patent. The phrase "configuration memory" appears in claim 14 of the '869 patent; claims 6, 23, 31, and 48 of the '795 patent; and claims 1 and 11 of the '107 patent. The phrases are used consistently in each patent and are meant to have a similar meaning. The parties do not dispute this as evidenced by their proposed constructions. In addition, the terms are not explicitly defined in the claims. Thus, the Court turns to the specification.

The glossary of the patent specification provides explicit definitions for the phrases "configuration register" and "configuration memory." Specifically, the glossary defines "configuration memory" to mean "the configuration memory contains one or more configuration

strings." '795 patent, 15:9-10; '107 patent, 15:16-17. The glossary also defines "configuration register" to "[t]he function to be carried out by the configurable element is entered into this register." '520 patent, 2:6-7; '998 patent, 2:31-32. Given these explicit definitions provided by the patentee, the Court adopts these definitions as its construction.

Regarding the phrase "configuration register," the specification of the '520 patents states:

> The present invention includes a run-time programmable, run-time reconfigurable unit. The configurable elements on the chip have one or more ***configuration registers*** for different tasks. Read and write access to these ***configuration registers*** may be provided. In describing the present invention, it is assumed that a configuration can be set in an element to be configured for the following information: Interconnection register. The type of connection with other cells is set in this register. Command register. The function to be carried out by the configurable element is entered in this register. Status register. The cell stores its current status in this register. This status provides information to the other elements of the component regarding which processing cycle the cell is in.

'520 Patent, 1:63-2:12 (emphasis added). In describing the configuration register, the specification generally describes a register that stores the configuration information of a cell. The parties' proposed construction confirms that they agree on this aspect of the configuration register. Plaintiff's proposed construction, however, adds the terms "dedicated" implying that the configuration register only stores configuration information and nothing else. Having carefully reviewed the intrinsic evidence, the Court finds no support for Plaintiff's proposed construction. The specifications of the '520 and '998 patents never mention the word "dedicated" or imply that the configuration registers store only configuration information and nothing else. (*See, e.g.,* '998 patent 2:23-28, 5:18-23; '520 patent 1:54-2:3, 2:12-17.) Furthermore the word "dedicated" in Plaintiff's construction is imprecise and would only

confuse the jury. Therefore, the Court adopts Defendants' proposed construction for this phrase as indicated in the table above.

6. "State Machine"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"State Machine"	Logic which can assume various states and the transitions between the states depend on various input parameters	logic which can assume miscellaneous states. The transitions between states depend on various input parameters. These machines are used to control complex functions and belong to the related art.

To begin its analysis, the Court first turns to the language of the claims. The disputed phrase "state machine" appears in claims 1, 5, 6, 9, 15, 16, and 18 of the '242 patent; claims 1 and 2 of the '181 patent; and claims 3 and 4 of the '106 patent. The phrase is used consistently in each patent and is meant to have a similar meaning. The parties do not dispute this as evidenced by their proposed constructions. In addition, the phrase is not explicitly defined in the claims. Thus, the Court turns to the specification.

The glossary of the patent specification provides explicit definitions for the phrase "state machine." Specifically, the glossary defines "state machine" to mean "logic which can assume miscellaneous states. The transitions between states depend on various parameters. These machines are used to control complex functions and belong to the related art." '181 patent 12:1-4; '106 patent 15:50-54; '077 patent 15:51-55. The only dispute between the parties is whether to include the last sentence of the definition. Defendants contend that it should be included because it illustrates to the jury that Plaintiff did not invent state machines. But, as previously noted, the parties have agreed to constructions that do not include the entire definition of the

term or phrase provided in the specification. For instance, the parties agreed construction for the terms "DPGA" and "FPGA" omits the parenthetical "(related art)." As with these terms, omitting the "and belong to the related art" portion of the explicit definition avoids any potential jury confusion. Obviously, the patentee described the claimed state machines as belonging to the related art, but this does not require including this description in the Court's construction. For these reasons, the Court construes "state machine" as "logic which can assume miscellaneous states. The transitions between states depend on various input parameters. These machines are used to control complex functions."

7. "Regrouping/Regrouped"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Regrouping"	Group again	forming a new collection of objects considered together
"Regrouped"	Group again	forming a new collection of objects considered together

The Court construes "regrouping" as "forming a new collection of cells," and "regrouped" as "having formed a new collection of cells."

A. Parties' Construction Arguments

The parties dispute whether changing function or interconnection is sufficient for a "regrouping" of cells. Plaintiff contends that the terms should be construed to mean "group again." Defendants contend that the term should be construed as "forming a new collection of objects considered together."

B. Analysis

To begin its analysis, the Court turns to the claims themselves. The disputed terms

"regrouping" and "regrouped" appear in claims 1, 5, 6, 9, 15, 16, 18 of the '242 patent; and claims 55 and 56 of the '869 patent. Claim 1 of the '242 patent recites:

> an integrated circuit data flow processor, said data flow processor including a plurality of cells arranged in a pattern having two or more dimensions, a plurality of connecting lines disposed between each said cells and a plurality of input and output ports, said cells connected to neighboring cells by a plurality of first data connections, said cells also connected to said connecting lines by a plurality of second data connections, at least some of said cells being selectively ***configured*** to perform ***a first function***, the at least some of said cells being selectively ***reconfigured*** to perform a ***second function***, the second function being different than the first function, the at least some of said cells being selectively ***grouped*** with another of said cells into functional parts by means of said first and second data connections to perform a ***third function***, the at least some of said cells being selectively ***regrouped*** to perform a fourth function, the fourth function being different than the third function, said cells connected to said input and output ports;

The Court first notes that the claim language does not use the term reconfigured and regroup interchangeably. Thus, the claim language draws a distinction between "reconfiguring" and "regrouping." Plaintiff's proposed construction fails to capture the distinction and is therefore rejected by the Court. Plaintiff argues that "there is nothing in the intrinsic evidence that suggests that a regrouping must involve new cells or a new number of cells." In other words, Plaintiff argues that the act of reconfiguring the cells in a group that were previously performing one function such that the same cells now perform another common function would also constitute a "regrouping." But this is not supported by the plain language of the claims, because this would be reconfiguring the same cells to perform another function and not regrouping the cells. For example, claim 1 of the '242 patent recites:

> a compiler configuring and reconfiguring selected ones of the at least some of said cells and selectively ***grouping and regrouping*** said selected ones of the at least some of said cells into functional

> parts as a function of the synchronization signals providing various logic functions and data manipulations among said cells and said functional parts to be realized, said compiler ***reconfiguring and regrouping*** said selected ones of the at least some of said cells during operation of said data flow processor while simultaneously others of the at least some of said cells not being ***reconfigured or regrouped*** process data.

Again, the claim language draws a distinction between "reconfiguring" and "regrouping," and Plaintiff's proposed construction fails to capture the distinction. Accordingly, the Court construes "regrouping" as "forming a new collection of cells," and "regrouped" as "having formed a new collection of cells."

8. "Processing Array Elements"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Processing Array Elements"	Configurable elements arranged systematically in rows and columns that perform operations on data"	EALU with O-REG, RREG, R2OMUX, F-PLUREG, MPLUREG, BM UNIT, SM UNIT, sync UNIT, state-back UNIT and power UNIT

The Court construes "Processing Array Elements" as "EALU with O-REG, RREG, R2OMUX, F-PLUREG, MPLUREG, BM UNIT, SM UNIT, Sync UNIT, State-back UNIT and power UNIT."

A. Parties' Construction Arguments

The parties dispute whether "PAE" is an acronym for "processing array element." Plaintiff contends that the glossary entry defines a "PAE" as a special type of "processing array element" that includes an "EALU" and other specialized components. In other words, Plaintiff argues that the glossary does not define a "processing array element."

B. Analysis

To begin, the Court first turns to the language of the claims. The phrase "processing array elements" appears in claims 4, 7, 8, 12 of the '871 patent. Two things are evident from the claim language. First, the phrase is used consistently in each claim. Second, the phrase is not explicitly defined in the claims. Thus, the Court turns to the specification.

As with a number of the disputed terms, the patent specification includes a glossary that explicitly defines the phrase "PAE." Specifically, the glossary of the '871 patent defines the phrase "PAE: processing array element:" as "EALU with O-REG, RREG, R2OMUX, F-PLUREG, MPLUREG, BM UNIT, SM UNIT, sync UNIT, state-back UNIT and power UNIT." '871 patent 17:64-67. Plaintiff contends that the use of the double colon in the definition indicates that the glossary entry defines a "PAE" as a special type of "processing array element" that includes an "EALU" and other specialized components. In other words, Plaintiff argues that the glossary does not define a "processing array element." The Court rejects this argument and adopts the explicit definition provided by the specification. To be sure, the specification also states that:

> ***The present invention*** relates to the design of a cell (e.g., ***processing array element or "PAE"***) as described in German Patent No. 44 16 881, or, for example, conventional FPGA cells, where the PAEs can be cascaded to form an array (e.g., a processing array or "PA"). One PAE is composed of a plurality of function units.

'871 patent, 3:33-37 (emphasis added). The specification goes on to describe the function units that are included in the PAE. '871 Patent, 3:38-7:42. These function units include the ALU with O-REG, RREG, R2OMUX, F-PLUREG, MPLUREG, BM UNIT, SM UNIT, Sync UNIT, State-back UNIT and Power UNIT provided in the explicit definition. Thus, the Court rejects

Plaintiff's argument and adopts the explicit definition provided by the patentee.

This conclusion is further confirmed by reviewing the explicit definition of "EALU" and "ALU" provided in the specification. The specification defines an "ALU" as "Arithmetic and logic unit. Basic unit for processing data. The unit can perform arithmetic operations such as addition, subtraction, or, under some circumstances, multiplication, division, series expansions, etc. The unit may be designed as an integer unit or as a floating point unit. It may also perform logic operations such as AND, OR, and comparisons." '871 Patent, 16:43-49. The specification defines "EALU" as "Expanded arithmetic and logic unit. An ALU expanded to add special functions that are needed or appropriate for the operation of a data processing system according to DE 44 16 881 A1. These are counters in particular." '871 Patent, 17:1-5. Thus, the specification make clear that the processing array element is an expanded arithmetic and logic unit (ELAU) including all of the function units listed in the explicit definition provided by the patentee. Accordingly, the Court construes "Processing Array Elements" as "EALU with O-REG, RREG, R2OMUX, F-PLUREG, MPLUREG, BM UNIT, SM UNIT, Sync UNIT, State-back UNIT and power UNIT."

9. "EALU"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"EALU"	An expanded arithmetic and logic unit that can perform arithmetic and logical operations, as well as counter functions"	Expanded arithmetic and logic unit. An ALU expanded to add special functions which are needed or appropriate for the operation of a data processing system according to German Patent No. 44 16 881. These are counters in particular.

The Court construes "EALU" as "Expanded arithmetic and logic unit. An ALU expanded to add special functions which are needed or appropriate for the operation of a data processing system according to German Patent No. 44 16 881. These are counters in particular."

A. Parties' Construction Arguments

The parties dispute whether the explicit definition provided by the specification should be modified to add the phrase "can perform," as well as limiting the "special functions" to "arithmetic and logical operations, as well as counter functions," as proposed by Plaintiff.

B. Analysis

To begin its analysis, the Court first turns to the language of the claims. The term "EALU" appears in claim 7 of the '871 patent. Again, the phrase is used consistently throughout the claim and is not explicitly defined in the claim. Thus, the Court turns to the specification.

As with a number of the disputed terms, the patent specification includes a glossary that explicitly defines the phrase "EALU." Specifically, the glossary defines "EALU" to mean "Expanded arithmetic and logic unit. An ALU expanded to add special functions that are needed or appropriate for the operation of a data processing system according to DE 44 16 881 A1. These are counters in particular." '871 Patent, 17:1-5. Thus, as defined by the patentee, an EALU is an arithmetic and logic unit (ALU) "expanded to add special functions." These special functions are not limited to only counting functions, but may include other arithmetic and logic operations. For example, the '871 patent specification states:

> EALU: The computing unit includes an expanded arithmetic and logic unit (EALU) permanently implemented in the logic unit. An EALU is an ordinary known arithmetic and logic unit (ALU) which has been expanded by special functions such as counters.

> This EALU is capable of performing a plurality of arithmetic and logic operations, which do not have to be specified here exactly, because it is possible to refer to known ALUs. The EALU has direct access to its own results (described below) which are returned as the operand. Thus counters or serial operations such as serial multiplication, division or series expansion are possible.

'871 patent, 3:39-50. Although the Court finds that the definition included in the glossary is the appropriate construction, the Court's construction does not limit the EALU to performing only counting functions. Accordingly, the Court construes "EALU" as "Expanded arithmetic and logic unit. An ALU expanded to add special functions which are needed or appropriate for the operation of a data processing system according to German Patent No. 44 16 881. These are counters in particular."

10. "Addressed/Addressable"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Addressed"	Capable of having data sent directly to it	capable of having data sent to it using a unique identifier
"Addressable"	Sent directly	Sent using a unique identifier

The Court construes "addressed" as "capable of having data sent to it using a unique identifier" and "addressable" as "sent using a unique identifier."

A. Parties' Construction Arguments

The dispute is whether the construction should include "a unique identifier" that requires each PAE to have a unique address. Plaintiff argues that Defendants' construction imports a limitation from the preferred embodiment into the claims.

B. Analysis

To begin its analysis, the Court first turns to the language of the claims. The term "addressable" appears in claim 1 of the '087 patent. The term "addressed" appears in claims 4, 7, 8, and 12 of the '871 patent. The terms are used consistently in each claim and are meant to have a similar meaning. Also, the terms are not explicitly defined in the claims. Moreover, claim 4 of the '871 patent contradicts Plaintiff's proposed construction. Specifically, claim 4 recites:

> A circuit, comprising:
> a plurality of coarse grained processing array elements;
> a primary logic unit ***communicatively coupled*** to the processing array elements; and
> an internal bus system;
> wherein ***each of the processing array elements*** is reconfigurable at a run time without effecting other processing array elements and without effecting data streams communicated between transmitters and receivers, by selecting one of a set of predefined, non-alterable instructions according to ***configuration data sent from the primary logic unit and addressed to the processing array element***, and each of the processing array elements is decoupled from the internal bus system.

As indicated by the claim, a primary logic unit is communicatively coupled to the processing array elements. These processing array elements receive configuration data from the primary logic unit that is addressed to the processing array element. Thus, the configuration data is not only sent directly to the processing array element, but is also "addressed" to the processing array element. In other words, the additional claim language of "addressed" would be superfluous if addressing only required send data directly.

Plaintiff relies heavily on arguments made during the prosecution of the '871 Patent to support its argument. Specifically, the patentee overcame a rejection by amending claim 1 such

that it recited: "A directly addressable configurable unit [with] directly addressable registers…." (Dkt. No. 140-27 at 25-26) (emphasis in original). The patentee further remarked that the "directly addressable" language required that the:

> PAEs themselves each have a unique address and that the PLU can send data directly to a specific PAE based on this address, and also that the registers F-PLUREG and MPLUREG of each PAE are equally directly addressable using the PAE address and a register select signal.

Id., at 31-32. Plaintiff argues that such a "directly addressable" configurable unit having PAEs with "unique addresses" was different from the prior art, which used an "implied addressing scheme" to send configuration data to the elements. *Id.* Thus, Plaintiff contends that the patentee drew a distinction in its claims that being "directly addressable" requires an explicit address, while the more generic "addressable"/"addressed" (as claimed by '871 claim 4 and '087 claim 1, for example) does not. The Court notes that claim 1 and claim 4 of the '878 patent are independent claims not of the same scope. Moreover, claim 4 was amended at the same time as claim 1 to include an "address" limitation. (Dkt. No. 140-27 at 27.) Granted, this amendment did not include the exact wording of "directly addressable," but it does include an "addressable" limitation. The Court agrees with Defendants that the prosecution history is ambiguous, and actually tends to suggest that the directly addressable or unique identifier limitation is required to avoid the prior art.

The Court further agrees that the patent specification supports Defendants' constructions of "having a unique identifier" and "sent using a unique identifier." The patents state that "[e]ach PAE has a ***unique address*** composed of its line and column within a PA (processing array)." '087 patent 9:36-37 (emphasis added). Furthermore, the patents state that there can be

"one SRAM address for each cell." *Id.* at 1:34-36. The patentee further explained that data can be directed to a particular cell using that cell's address, and the cell can choose to either ignore the data presented to it or not, depending on whether the data matches that cell's address. *See id.* at 9:32-46 ("The AX and AY addresses of the PLU bus (0308) are compared with the address of PAE in a comparator (0301) if AEN (address enable) indicates a valid bus transfer.").) Plaintiff does not dispute that this unique identifier is disclosed in the specification. The Court therefore adopts Defendants' construction.

11. "Configuration Control Terms"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Configuration unit"	No construction necessary; plain and ordinary meaning applies. Alternatively, "A component that configures another component"	A central unit for configuring and reconfiguring the PAEs or logic cells. Embodied by a microcontroller specifically designed for this purpose."
Court's Construction	Unit for configuring and reconfiguring a PAE or logic cell. Embodied by a microcontroller specifically designed for this purpose.	
"Reconfiguration unit""	No construction necessary; plain and ordinary meaning applies. Alternatively, "A component that reconfigures another component"	A central unit for configuring and reconfiguring the PAEs or logic cells. Embodied by a microcontroller specifically designed for this purpose
Court's Construction	Unit for configuring and reconfiguring a PAE or logic cell. Embodied by a microcontroller specifically designed for this purpose.	

"Primary logic unit"	A microcontroller specifically designed for configuring and reconfiguring another component"	A central unit for configuring and reconfiguring the PAEs or logic cells. Embodied by a microcontroller specifically designed for this purpose."
Court's Construction	Unit for configuring and reconfiguring a PAE or logic cell. Embodied by a microcontroller specifically designed for this purpose.	
"Primary function control unit"	A component for configuring and reconfiguring another component"	A central unit for configuring and reconfiguring the PAEs or logic cells. Embodied by a microcontroller specifically designed for this purpose."
Court's Construction	Unit for configuring and reconfiguring a PAE or logic cell. Embodied by a microcontroller specifically designed for this purpose.	
"Compiler	Unit that configures the arithmetic and logical operations of one or more individual cells"	A central unit for configuring and reconfiguring the PAEs or logic cells. Embodied by a microcontroller specifically designed for this purpose."
Court's Construction	Unit for configuring and reconfiguring a PAE or logic cell. Embodied by a microcontroller specifically designed for this purpose.	

The Court construes each of the disputed phrases as indicated in the table above.

A. Parties' Construction Arguments

The parties generally agree that "primary logic unit," "primary function control unit," "configuration unit," "reconfiguration unit," and "compiler" (collectively "the configuration control terms") are responsible for configuring and/or reconfiguring. This is because the patentee uses these configuration control terms interchangeably throughout the '871, '181, '087, '795, '869, and '242 patents. Defendants note that neither "configuration unit" nor "reconfiguration unit" appear in the specification, while "compiler" is discussed in some detail. (*See, e.g.*, '869 patent 6:22-34; *see also* Dkt. No 142-3, McAlexander Decl. at ¶ 146.) Thus, Defendants argue that the discussion of "compiler" serves as written description support for the

claim terms "configuration unit" and "reconfiguration unit" in the '869 patent. Notwithstanding, Plaintiff agrees that "configuration unit" and "reconfiguration unit" should be construed identically. In addition, Plaintiff's expert has recognized that the terms "compiler," "PLU," "configuration unit," and "reconfiguration unit" are interchangeable. *See* Dkt. No. 142-8, Tredennick Tr. at 131:24-132:2.

B. Analysis

To begin its analysis, the Court first turns to the language of the claims. The phrase "configuration unit" appears in claims 13, 14, 15, 17, 18, and 19 of the '869 patent; and claim 23 of the '795 patent. The phrase "reconfiguration unit" appears in claim 65 of the '869 patent. The phrase "primary logic unit" appears in claims 4, 7, 8, and 12 in the '871 patent; and claim 30 of the '181 patent. The phrase "primary function control unit" appears in claim 1 of the '087 patent. The term "compiler" appears in claims 1, 5-6, 9, 16 of the '242 patent; and claim 55 and 56 of the '869 patent. The phrases are used consistently in each patent and are meant to have a similar meaning. In addition, the terms are not explicitly defined in the claims. Thus, the Court turns to the specification.

The glossary of the patent specification provides an explicit definition for the phrase "primary logic unit." Specifically, the glossary of the '181 Patent defines a "Primary Logic Unit (PLU)" as "Unit for configuring and reconfiguring a PAE or logic cell. Embodied by a microcontroller specifically designed for this purpose." '181 patent, 11:31-34. Plaintiff argues that Defendants' construction of primary logic unit incorrectly adds limitations to this definition by requiring (1) that the primary logic unit must be "central" and (2) that the primary logic unit must be "embodied by a microcontroller." The Court agrees that Defendants' proposed

construction improperly adds "central" to the explicit definition provided by the patentee. Thus, the Court will not include it in its construction. The Court, however, disagrees that Defendants' proposed construction improperly includes "embodied by a microcontroller." This limitation is explicitly stated in the definition provided by the patentee in the specifications of the '181 patent. This definition explicitly references both the configuring PAE and logic cells. At the claim construction hearing, Plaintiff presented a compromise construction for "primary logic unit" that is consistent with the Court's findings. Moreover, the Court's construction is consistent with the intrinsic evidence.

To the extent that Plaintiff stands behind its original constructions, Plaintiff argues that the '181 specification teaches that the primary logic units may be composed of configurable logic cells and need not be "embodied by a microcontroller":

> "The following description encompasses several architectures which may be controlled and configured by a primary logic unit, as in DFPs, FPGAs, DPGAs, etc. Parts of the primary logic unit may be integrated on the unit. As an alternative, there is the possibility (FIGS. 6, 7) of dynamically controlling or reconfiguring the architectures directly through the unit itself. The architectures may be implemented in a permanent form on the unit, or they may be created only by configuring and possibly combining multiple logic cells, i.e., configurable cells which fulfill simple logical or arithmetic functions according to their configuration (cf. DFP, FPGA, DPGA)."

'181 patent, 2:23-34. The Plaintiff also correctly notes that the '871 patent glossary states that the primary logic unit is "configured by a microcontroller adapted specifically to its task," instead of "embodied as a microcontroller." '871 18:1-3. The problem with Plaintiff's argument is that the patents do not disclose a microcontroller that configures the primary logic unit. Instead, the patents disclose that the primary logic unit is the unit that is specifically designed for

the purpose of configuring and reconfiguring a PAE or logic cell. Therefore, the Court construes the configuration control terms as indicated in the table above.

12. "Coarse Grained"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Coarse Grained"	Implements only word-level operations and reconfigured only at the word-level	Something that operates on more than one bit at a time

The Court construes "coarse grained" as "something that operates on more than one bit at a time."

A. Parties' Construction Arguments

The dispute is whether coarse grained requires: (1) the multiple bits being operated on must be "treated as a 'word,'" and (2) if a coarse-grained element must be "reconfigured only at the word-level."

B. Analysis

To begin its analysis, the Court turns to the claims themselves. The phrase "coarse grained" appears in claims 4, 7, 8, and 12 of the '871 patent. Claim 4 recites a circuit that includes "a plurality of coarse grained processing array elements." The claim language does not provide much insight on the meaning of the term. Thus, the Court next turns to the specification.

Plaintiff contends that what distinguishes "coarse grained" from "fine grained" is not whether the element operates on a single bit, but rather whether it operates on multiple bits treated as a "word" and is reconfigured only at the word-level. To support this position, Plaintiffs contend that the specification of the '871 patent teaches that the PAEs are "coarse

grained" under PACT's construction. For example, Figures. 5b and 7b in the '871 patent, in combination with Figure 2, show that EALU 208 within the PAE inputs only an n-bit word of data from either O-REGsft 204 or R->O MUX 206. Defendants respond that these are not example of the patent restricting "coarse grained" to "words," but are descriptions of multiplexers and registers capable of operating on multiple bits. Defendants also contend that the construction of "reconfigured at the word level" is not supported by the intrinsic evidence because the file history refers only to how a unit "operates," not how it is reconfigured. (Dkt. No. 142-26 at 8.) Plaintiff argues that because "the PAEs must implement word-level operations," it follows that "the PAE is reconfigured only at the word level." (Dkt. No. 140 at 34-35.) The Court agrees that the Plaintiff offers no persuasive support for this explanation.

Further, Defendants point to the remarks made by the patentee's during the prosecution of U.S. Patent No. 7,565,525 ("the '525 patent"), which is a continuation application of the '871 patent, to support its construction. *See, e.g., Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1353 (Fed. Cir. 2005) (noting that the prosecution history of a continuation application is "relevant material that [the court] should consider."). Specifically, the examiner rejected claims in the '525 patent application containing the term "coarse grain unit" for "failing to comply with the written description requirement." (Dkt. No. 142-26 at 12-13.) In response, the patentee removed the term from those particular claims, and explained that "one skilled in the art would recognize that coarse grained units refer to processing units at a higher than micro level, e.g., higher than the gate level, such as an ALU. For example, in contrast to a coarse grained unit, a unit that can operate at only one bit at a time operates at the gate level." (*Id.* at 8.) The patentee is making the distinction between coarse grain and fine grain based on the level that the

operation occurs, not on the level it is configured. Based on the intrinsic evidence, the Court agrees with Defendant and construes "coarse grained" as "something that operates on more than one bit at a time."

13. "Haltered or Impaired"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Haltered or Impaired"	Disabled or negatively affected	affected or disabled

The Court construes "Haltered or Impaired" as "disabled or deactivated"

A. Parties' Construction Arguments

The dispute is whether the phrase "haltered or impaired" connotes negative consequences, as Plaintiff suggests, or is neutral as to the effect of being "haltered or impaired," as Defendants suggest. Both parties include the concept of "disabled" in their constructions of this term. Plaintiff contends that Defendants' construction improperly permits a cell to be "haltered or impaired" if it is merely "affected."

B. Analysis

To begin its analysis, the Court turns to the claims themselves. The disputed phrase "haltered or impaired" appears in claim 13, 14, 15, and 17 of the '869 patent. Claim 13 recites that "the at least some of the plurality of computing cells being configured as a function of the at least one configuration signal during operation of the massively parallel data processing apparatus such that others of the plurality of computing cells not being configured are not ***haltered or impaired*** in their operations." The term "haltered" does not appear anywhere else in the specification of the '869 patent. The term "impaired" does appear in the abstract, which states that "[t]he manipulation of the DFP configuration is performed during DFP operation such

that modification of function parts (MACROs) of the DFP can take place without requiring other function parts to be ***deactivated or being impaired***." Based on the intrinsic evidence the Court construes "haltered or impaired' to mean "disabled or deactivated." The Court is of the opinion that "affected" can mean many different things as indicated by the parties' dispute surrounding this term. Therefore, including "affected" or "negatively affected" in the construction would not provide any guidance for the jury and is not necessary to properly construe the term.

14. "Bundled"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Bundled"	Combined	physically routed together

The Court construes "bundled" as "combined."

A. Parties' Construction Arguments

The dispute is whether this term should be limited to "physical bundling," which requires physical proximity among the objects, or whether it can also encompass "logical bundling," which does not require physical proximity.

B. Analysis

To begin its analysis, the Court first turns to the language of the claims. The term "bundled" appears in claims 1, 2, 3-5, and 17 of the '181 patent; claims 2-4, 8, and 13 of the '106 patent; and claim 1 of the '077 patent. Two things are evident from the claim language. First, the term is used consistently in each patent and is meant to have a similar meaning. The parties do not dispute this as evidenced by their proposed constructions. Second, the term is not explicitly defined in the claims. Thus, the Court examines the specification.

The specification of the '181 patent describes "Bundling Internal Lines" where the "lines may be internal bus systems or lines of the edge cells." '181 patent, 2:35-39. Thus, the specification contemplates both "physical bundling" and "logical bundling" because internal bus systems can be bundled with lines of the edge cells. Therefore, the Court rejects Defendants construction that includes only physical bundling and adopts Plaintiff's construction that includes both physical and logical bundling. The Court has reviewed the prosecution history and finds Defendants' arguments relating to this intrinsic evidence unpersuasive.

15. "Ordinary connections in a manner customary with at least one of the DFP, the FPGA and the DPGA"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Ordinary connections in a manner customary with at least one of the DFP, the FPGA and the DPGA"	"Single, unrelated wires whose function is configured by the DFP, FPGA or DPGA."	This term is indefinite, and as such no construction can be discerned.

The Court construes "ordinary connections in a manner customary with at least one of the DFP, the FPGA and the DPGA" as "single wires that are not bundled with the plurality of the at least one of individual lines, buses, and subbuses."

A. Parties' Construction Arguments

Defendants contend that the disputed phrase is indefinite because one of skill in the art would not be able determine whether particular "connections" meet the limitation. Specifically, Defendants argue that there is nothing in the intrinsic or extrinsic evidence supporting any standard for determining what is "ordinary" or "customary." *See Datamize, LLC* , 417 F.3d at 1350 (holding the term "aesthetically pleasing" to be indefinite because the claims and specification offered no objective standard to measure "aesthetically pleasing").

B. Analysis

To begin its analysis, the Court turns to the claims themselves. The disputed phrase "ordinary connections in a manner customary with at least one of the DFP, the FPGA and the DPGA" appears in claim 1 of the '077 patent. Claim 1 of the '077 patent recites:

> 1. A bus system, comprising:
> a plurality of at least one of individual lines, buses, and subbuses within at least one of a unit including at least one of a data flow processor (DFP), a field programmable gate array (FPGA), a dynamically programmable gate array (DPGA), and a unit having a multi-dimensional programmable cell architecture, the plurality of the at least one of individual lines, buses and subbuses being bundled,
> wherein the plurality of the at least one individual lines, buses and subbuses at least one of combines multiple units and connects at least one of memories and peripherals, and wherein standard bus systems are used, and
> wherein the unit includes additional **ordinary connections in a manner customary with at least one of the DFP, the FPGA and the DPGA**.

Bases on this claim language, Plaintiff contends that Figure 12 describes the claimed "ordinary connections" that were customary to the DFP, FPGA or DPGA:

> "FIG. 12 shows an example embodiment using a standard bus system RAMBUS (1203). One unit (DFP, FPGA, DPGA, etc.) (1201) is connected to other units (memories, peripherals, other DFPs, FPGAs, DPGAs, etc.) (1202) by the bus system (1203). IO dependently of the bus system (1203), this unit (1201) may have additional connecting lines (1204), e.g., for connecting any desired circuits, as is customary in the related art."

'077 10:65-11:5. From this Plaintiff concludes that the claimed "ordinary connections" are separate and distinct from the claimed plurality of "individual lines, busses and subbusses" 1203 that are "bundled" and either "combine multiple units" 1202 or "connects [] memories and

peripherals" 1202. *Id.*; *see* '077 claim 1. Plaintiff also argues that a person of ordinary skill knew that such ordinary and customary connections in conventional DFPs FPGAs, and DPGAs were "single, unrelated wires whose function [was] configured by [either] the DFP, FPGA or DPGA," depending on the device. Tredennick Decl., ¶ 129. The Court agrees, in part, with Plaintiff and construes "ordinary connections in a manner customary with at least one of the DFP, the FPGA and the DPGA" as "single wires that are not bundled with the plurality of the at least one of individual lines, buses, and subbuses."

16. "Synchronization Vector"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Synchronization vector"	"An array of synchronization signals"	"Synchronization signals representing the result of a comparison"

The Court construes "synchronization vector" as "an array of synchronization signals representing the result of a comparison."

A. Parties' Construction Arguments

The parties agree that a synchronization vector consists of multiple synchronization signals. The dispute is whether the term "synchronization vector" is an array or represents the result of a comparison.

B. Analysis

To begin its analysis, the Court first turns to the language of the claims. The disputed phrase "synchronization vector" appears in claims 21 and 22 of the '998 patent. The phrase is used consistently throughout the claims, and the term is not explicitly defined in the claims.

Thus, the Court turns to the specification.

The phrase "synchronization vector" does not appear in the specification of the '998 patent. Instead the specification refers to a "trigger vector" and states that the trigger vector is a result of a comparison. '998 patent, 9:66 ("trigger vectors (i.e. the results of the comparison)", 6:54-55 ("trigger vectors generated by other processes on the basis of comparisons.") Thus, when the specification discusses a "vector," it describes it as a result of a comparison. *See, e.g.*, '998 patent, 5:3-11 ("trigger vector can therefore assume the states 'equal,' 'greater' or 'less'"), 5:12-23, 9:15-10:59 ("0501 generates by comparison a trigger vector").

Plaintiff contends that the term "synchronization vector" refers to an array of synchronization signals based on the use of the term in claim 38 of the '998 patent, which recites "the synchronization signal is part of a synchronization vector comprising a plurality of synchronization signals." Plaintiff also contends that plain and ordinary meaning of "vector" is a one-dimensional array. After reviewing the intrinsic evidence, the Court construes the phrase "synchronization vector" to mean "an array of synchronization signals representing the result of a comparison." This construction is consistent with the intrinsic evidence and the plain and ordinary meaning of the term "vector."

17. "Position Pointer/Pointer"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Position Pointer/Pointer"	"An identifier that specifies the location of data in storage"	"Address of the current record for read/write access within a FIFO or a ring memory"

The Court construes "position pointer/pointer" as "address of the current record for read/write access within a memory."

To begin its analysis, the Court first turns to the language of the claims. The phrases "position pointer" and "pointer" appear in claims 6, 31, 48, and 49 of the '795 patent; and claims 1 and 11 of the '107 patent. Two things are evident from the claim language. First, the phrases are used consistently in each patent and are meant to have a similar meaning. Second, the terms are not explicitly defined in the claims. Thus, the Court next turns to the specification.

The glossary of the patent specification provides explicit definitions for the phrases "read position pointer" and "write position pointer." Specifically, the glossary defines "read position pointer" as "[a]ddress of the current record for read access within a FIFO or a ring memory," and "write position pointer" as "[a]ddress of the current record for write access within a FIFO or ring memory" '795 Patent, 15:5-56. Plaintiff contends the claims recite a "pointer" and a "position pointer," which are not the same as the "read position pointer" and "write position pointer" described in the preferred embodiment. Plaintiff argues that it would it is improper to limit the constructions of a "pointer"/"position pointer" to the glossary entries for "read position pointer" and "write position pointer" that recite addresses, records for read/write access and FIFOs or ring memories. The Court notes that glossary terms do not further limit the phrase "position pointer," but instead simply indicate whether the position pointer is a read pointer or a write pointer.

Next, Plaintiff argues that the claims specify that the "pointer"/"position pointer" is used with a "configuration memory" or a "table [of] configuration strings" – not with just a "FIFO or a ring memory" as in the preferred embodiment. The Court agrees and finds that Defendants proposed construction improperly reads a preferred embodiment into the claim language. That is, Defendants proposed construction limits the claims to only to a FIFO or a ring memory. Thus, in light of the intrinsic evidence, the Court construes "position pointer/pointer" as "address of the

current record for read/write access within a memory."

18. "Event"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"Event"	No construction necessary; plain and ordinary meaning applies. In the alternative, "An occurrence or happening"	"Occurrence or happening reported by a functional element. An event can be analyzed by a hardware element in any manner suitable for the application and trigger an action as a response to this analysis."

The Court construes "event" as "an occurrence or happening that triggers an action."

To begin its analysis, the Court first turns to the language of the claims. The term "event" appears in claims 6, 8, 23, 31, 48, 49 of the '795 patent; and claims 1 and 11 of the '107 patent. The term is used consistently in each patent and is meant to have a similar meaning. Moreover, the term is not explicitly defined in the claims. Thus, the Court turns to the specification.

The glossary of the patent specification provides explicit definitions for the term "event." Specifically, the glossary defines "event" to mean "an event can be analyzed by a hardware element in any manner suitable for the application and trigger an action as a response to this analysis." '795 patent, 14:43-48. The definition goes onto provide specific examples of events. It appears that both parties agree that the examples provided in the glossary definition should be left out of the construction because they might confuse the jury. Additionally, Defendants have incorporated the Plaintiff's proposed construction "occurrence or happening" into this explicit definition to resolve any dispute that the glossary definition does not directly define event. Plaintiff disagrees that this resolves the dispute because it also includes "reported by a function

element" into the construction. The Court agrees that claim 1 of the '107 patent already recites "reported by a function element" and this would be redundant. Therefore, the Court construes "event" to mean "an occurrence or happening that triggers an action."

19. "Configuration/Reconfiguration Data"

Claim Term or Phrase	PACT's Proposed Construction	Xilinx's & Avnet's Proposed Construction
"configuration data"	"data used for configuring" (construction for '871 claims) "any set of configuration strings" (construction for '795 claims)	"any set of configuration strings"
"reconfiguration data"	"data used for reconfiguring"	"any set of configuration strings used for reconfiguring"

The Court construes "configuration data" as "any set of configuration strings," and "reconfiguration data" as "any set of configuration strings used for reconfiguring."

A. Parties' Construction Arguments

The only substantive difference in the parties' constructions is whether "configuration data" and "reconfiguration data" as claimed by the '871 and '869 can consist of a single "configuration string," as Plaintiff contends, or whether it must contain a set of "configuration strings."

B. Analysis

To begin its analysis, the Court first turns to the language of the claims. The disputed phrase "configuration data" appears in claims 48 and 49 of the '795 patent; and claims 4, 7, and 8 of the '871 patent. The disputed phrase "reconfiguration data" appears in claim 55 and 56 of the '869 patent. The phrases are used consistently in each patent and are meant to have a similar

meaning. And, the phrases are not explicitly defined in the claims. Thus, the Court next turns to the specification.

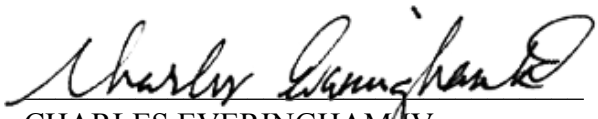
The glossary of the patent specification provides an explicit definition for the term "configuration data." Specifically, the glossary defines "configuration data" as "[a]ny set of configuration strings." '795 patent, The Court therefore adopts the explicit definition provided by the patentee.

Regarding the phrase "reconfiguration data," the Court finds Plaintiff's argument unpersuasive. Contrary to Plaintiff's assertions, claim 54 of the '869 patent does not teach sending "reconfiguration data" to a single cell. Instead, claim 54 requires that the "at least one of the cells" is regrouped "as a function of reconfiguration data." '869 patent claim 54. Thus, consistent with the explicit definition of the phrase "configuration data," the Court construes "reconfiguration data" to mean "any set of configuration strings used for reconfiguring."

VI. CONCLUSION

The Court adopts the constructions set forth in this opinion for the disputed terms and disputed phrases of the patents-in-suit. The parties are ordered that they may not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties are ordered to refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by the Court.

SIGNED this 17th day of June, 2011.



CHARLES EVERINGHAM IV
UNITED STATES MAGISTRATE JUDGE